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Current-Mode Controlled DC-DC Regulators (Part 4): Small-Signal Behavior Of The CC Loop

by Timothy Hegarty, Texas Instruments, Phoenix, Ariz.

This article, part 4 of a multipart series, considers a dc-dc regulator with constant-current (CC) or constant-voltage (CV) output regulation, depending on the operating condition and application requirement. In particular, this installment examines the small-signal behavior of the CC loop and its compensation.

In part 1, I reviewed the small-signal behavior[1] of the CV loop, including considerations for slope compensation, and presented the control-to-output transfer function for a buck regulator. In part 2, I examined a compensation design[2] for the CV loop, while simultaneously optimizing the load transient performance. Part 3 outlined incumbent solutions[3] for the CC circuit, but these were quite cumbersome, essentially requiring modification of a CV regulation scheme by supplementing the feedback loop with external circuits.

This led to the definition of a CC-CV regulator with a novel dual-loop architecture[3] activating either the CC or CV error amplifier at a given time, thus minimizing loop interactions and yielding a seamless handoff from CC to CV and vice versa. I then described a synchronous buck controller with this CC-CV implementation (the LM5190-Q1) that offers accurate current-regulation performance, a low external component count and reduced cost.

This fourth installment builds on part 3 by pursuing the relevant small-signal transfer functions for the CC loop. Designing the CC and CV loops with similar small-signal dynamics enables the use of a shared compensation component network. Bode plot simulations of the loop response in CC mode, based on a commercially available CC-CV synchronous buck converter (the LMG708B0), illustrate the small-signal characteristics of the dual-loop architecture.

Review Of The Dual-Loop CC-CV Architecture

Fig. 1 shows a dc-dc regulator schematic using the LMG708B0 gallium nitride (GaN) synchronous buck converter[4] from Texas Instruments (TI). The integrated circuit (IC) incorporates the power switches, gate drivers, bootstrap circuit and a buck controller that includes CC-CV functionality.

As shown in Fig. 2 by the structural diagrams for the CV and CC loops of the converter, this implementation is unique to the LMG708B0 and the LM5190 in that it selects the minimum of the currents from the transconductance error amplifiers in the CV and CC loops. The minimum function block, designated as the IMIN selector and highlighted in red in Fig. 2, performs this function by selecting whichever error current is lower.

For example, the CC loop takes control when the IMIN selector directs the current from the current-loop error amplifier. The selected error current then flows in a shared Type II compensation network, the resultant compensation (COMP) voltage becoming the reference command of the inner current loop of the peak current-mode architecture. Only one error amplifier is active at a given time, thus minimizing loop interactions and yielding a clean transition and seamless hand off from CV regulation to CC and vice versa.

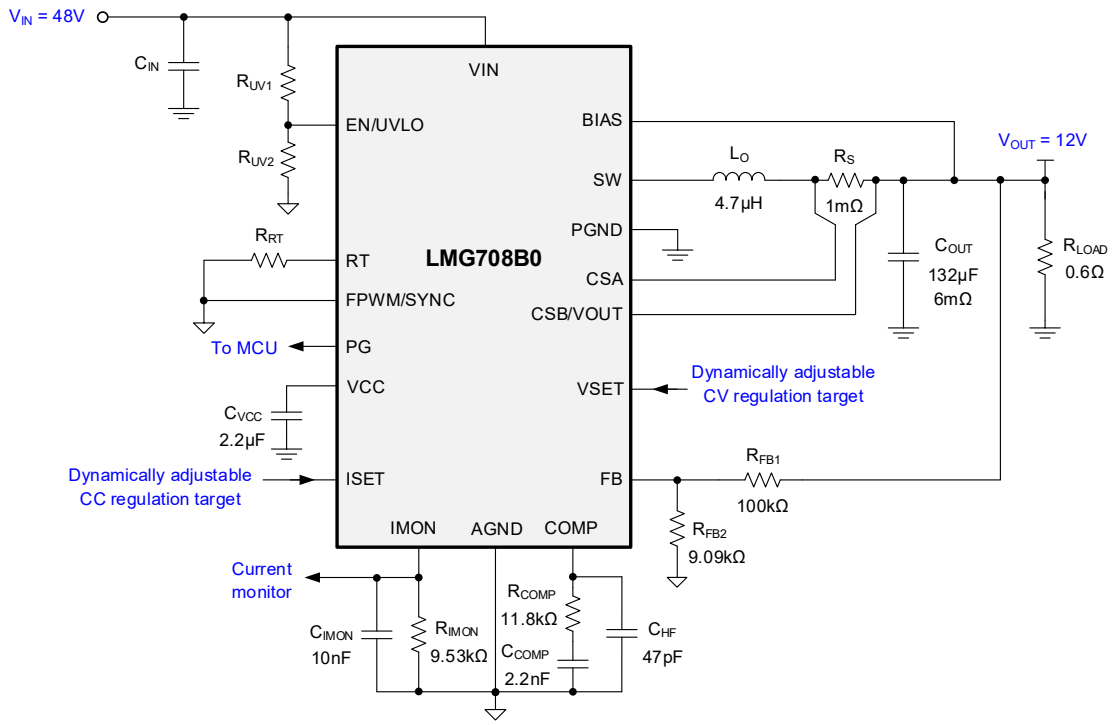

Fig. 1. Typical circuit schematic of a synchronous buck converter with CC-CV.

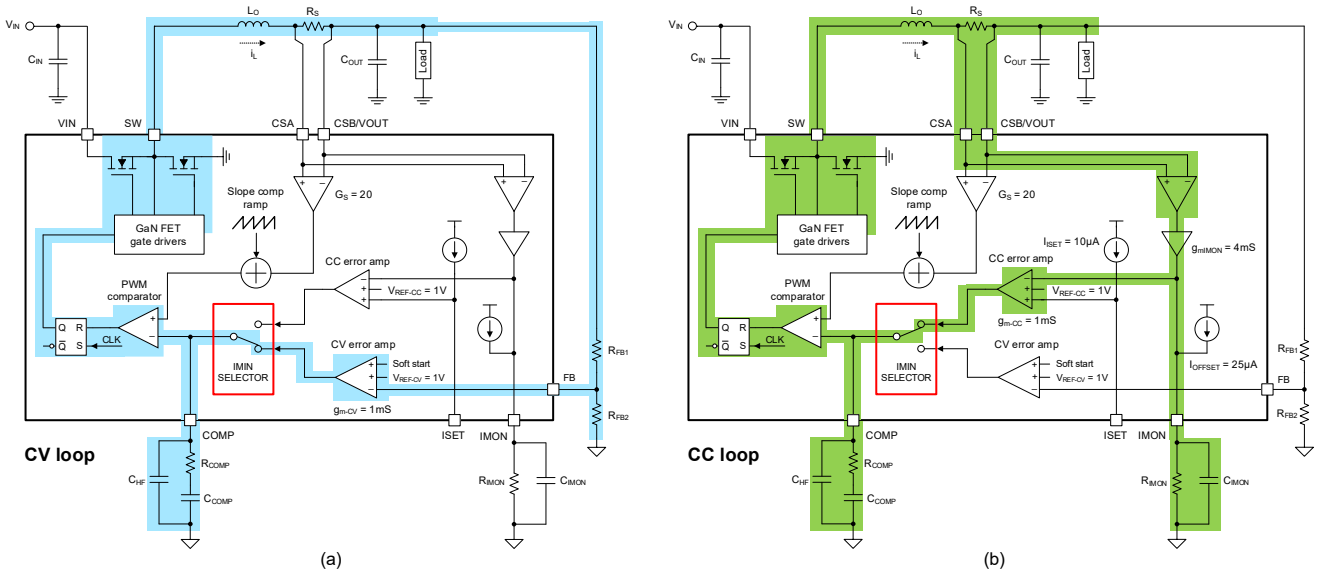

Fig. 2. Functional diagram of the buck converter highlighting the CV loop (a) and CC loop (b).

As highlighted in Fig. 2b, the CC loop requires just two external components connected at the IMON pin to establish the CC loop setpoint and CC loop stability. IMON acts as a monitor of the average inductor current and establishes a slower average current-limit function, which is typically set below the conventional instantaneous peak inductor current limit typically procured with peak current-mode control.

IMON sources a current proportional to the voltage sensed across the shunt, R_S. The CC loop starts to regulate the current when the IMON voltage reaches the 1-V reference of the current-loop error amplifier. For simplicity,

Fig. 2 does not highlight the peak current-mode inner loop—including the current-sense amplifier and slope compensation ramp—even though it is relevant for both CV and CC modes.

Designing The CC Loop

Based on the circuit in Fig. 2b, use equation 1 to select the IMON pin resistance for a given CC setpoint:

$$R_{imon} = \frac{V_{ref\text{-}CC}}{g_{m\text{-}imon} I_{out\text{-}CC} R_S + I_{offset}} \quad (1)$$

where $V_{ref\text{-}CC}$ = 1 V is the current-loop error amplifier reference voltage, $g_{m\text{-}IMON}$ = 4 mS is the IMON amplifier transconductance, and I_{offset} = 25 µA is the IMON offset current. Equation 2 extracts the output current from the IMON pin voltage as:

$$I_{out} = \frac{\left(V_{imon} / R_{imon}\right) - I_{offset}}{g_{m\text{-}imon} R_S} \quad (2)$$

A capacitor designated as C_{imon} in Fig. 2 removes the switching ripple to provide a representation of the average inductor current, which effectively corresponds to the output current.

Control Loop Block Diagram

Fig. 3 depicts the small-signal block diagram of the CC-CV system, where $v_{cs}(s)$ is the current-sense voltage and $v_{comp}(s)$ is the COMP voltage, the command for the inner peak current loop. Parameters $g_{m\text{-}CV}$ and $g_{m\text{-}CC}$ denote the voltage-loop and current-loop error amplifier transconductances, respectively. G_S is the current-sense amplifier gain, and $G_{imon}(s)$ is the current monitor gain.

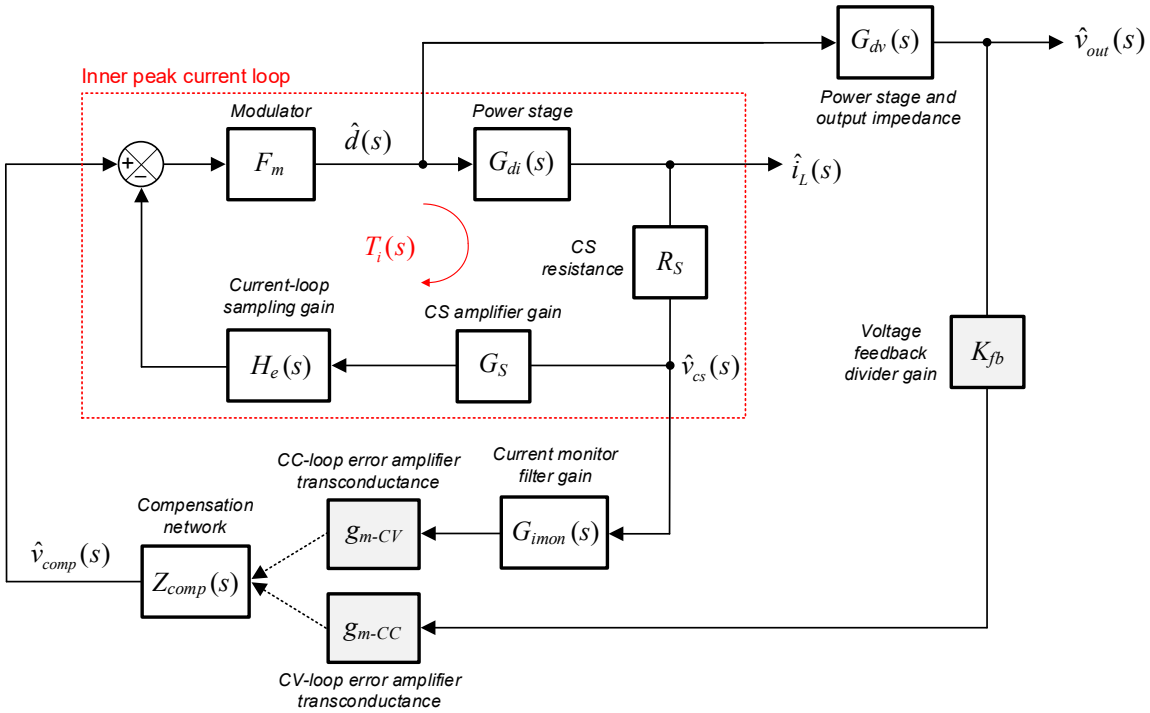

Fig. 3. Small-signal block diagram of the CC and CV loops in a peak current-mode architecture.

Deriving The CV Loop Transfer Function

To simplify Fig. 3, notice that the output impedance relates the duty-cycle-to-inductor-current and duty-cycle-to-VOUT transfer functions,

$$G_{di}(s) = \frac{G_{dv}(s)}{Z_{out}(s)} \tag{3}$$

For a purely resistive load,

$$Z_{out}(s) = R_{load}\frac{1+sR_{esr}C_{out}}{1+s\left(R_{load}+R_{esr}\right)C_{out}} = R_{load}\frac{1+\frac{s}{\omega_{\text{esr}}}}{1+\frac{s}{\omega_{p\text{-load}}}} \tag{4}$$

where the parameters $\omega_{p\text{-load}}$ and ω_{esr} are the load pole and output capacitor ESR zero, respectively.

Fig. 4 illustrates the small-signal block diagram of the CV loop, obtained by simplifying Fig. 3.

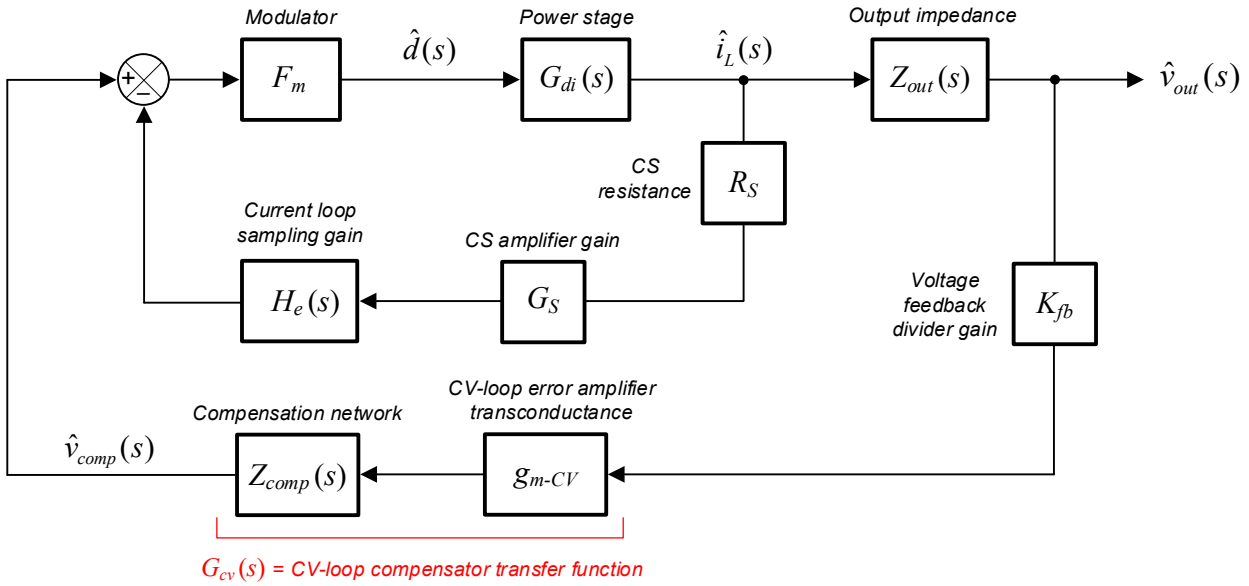

Fig. 4. Small-signal block diagram of the CV loop.

Recalling equation 2 from part 2, equation 5 expresses the VOUT-to-COMP (compensator) transfer function, including the gain K_{fb} from the feedback resistor divider network, as

$$G_{cv}(s) = \frac{\hat{v}_{comp}(s)}{\hat{v}_{out}(s)} = -K_{fb}g_{m\text{-}CV}Z_{comp}(s) \tag{5}$$

where $Z_{comp}(s) = \frac{1+sR_{comp}C_{comp}}{sC_{comp}\left(1+sR_{comp}\left(C_{hf}+C_{bw}\right)\right)} = \frac{1}{sC_{comp}}\frac{1+\frac{s}{\omega_{z\text{-}comp}}}{1+\frac{s}{\omega_{p\text{-}comp}}}$.

Recalling equation 10 from part 2, $G_{comp\text{-}to\text{-}vout}(s)$ is the COMP-to-VOUT (control-to-output voltage) transfer function derived in Ridley[2] and expressed as

$$G_{comp\text{-}to\text{-}vout}(s)=\frac{R_{load}}{R_i k_d}\frac{1+sR_{esr}C_{out}}{1+s\frac{R_{load}C_{out}}{k_d}}\frac{1}{1+\frac{s}{Q\omega_n}+\frac{s^2}{\omega_n^2}}=A_{comp\text{-}to\text{-}vout}\frac{1+\frac{s}{\omega_{esr}}}{1+\frac{s}{\omega_p}}H(s) \qquad (6)$$

where $A_{comp\text{-}to\text{-}vout}=\frac{R_{load}}{R_i k_d}$.

$H(s)$, defined in part 2 as the high-frequency extension in the COMP-to-VOUT transfer function designed to model the modulator sampling gain, is a pair of complex poles at half the switching frequency.

Fig. 5 shows the COMP-to-VOUT transfer function for the converter in Fig. 1, where the CV setpoint is 12 V and the load is 20 A.

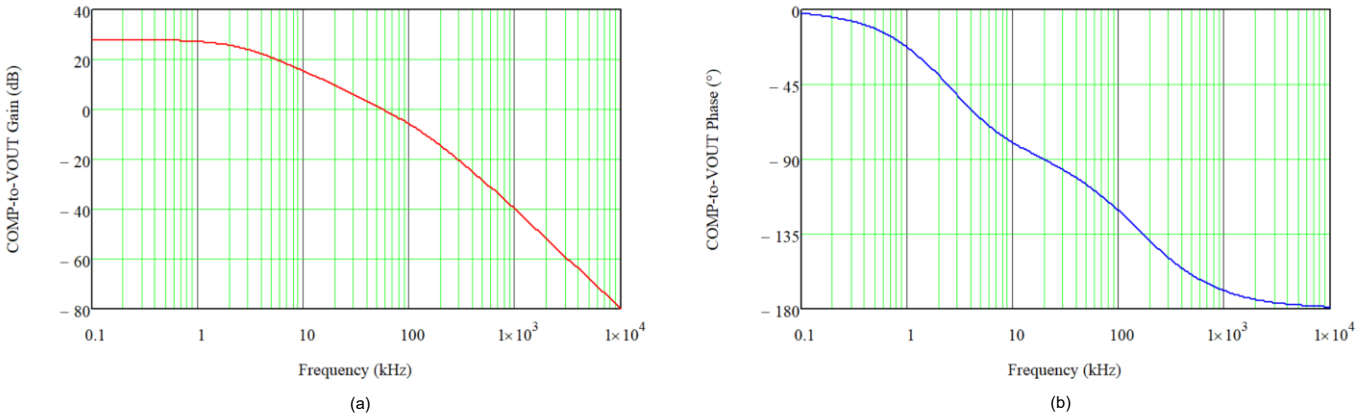

Fig. 5. Magnitude (a) and phase (b) of the COMP-to-VOUT response, $G_{comp\text{-}to\text{-}vout}(s)$.

The CV loop gain is the product of the VOUT-to-COMP (compensator) and COMP-to-VOUT (plant) transfer functions,

$$T_{cv}(s)=G_{cv}(s)G_{comp\text{-}to\text{-}vout}(s)=-K_{fb}g_{m\text{-}CV}Z_{comp}(s)\cdot\left[A_{comp\text{-}to\text{-}vout}\frac{1+\frac{s}{\omega_{esr}}}{1+\frac{s}{\omega_p}}H(s)\right] \qquad (7)$$

Equation 8 reduces the dc gain terms in equation 7 to

$$A_{cv}=K_{fb}g_{m\text{-}CV}A_{comp\text{-}to\text{-}vout}=K_{fb}g_{m\text{-}CV}\frac{R_{load}}{R_i k_d}=\frac{V_{ref\text{-}CV}}{V_{out}}g_{m\text{-}CV}\frac{R_{load}}{R_i k_d}=\frac{g_{m\text{-}CV}}{R_i k_d}\frac{V_{ref\text{-}CV}}{I_{out\text{-}CV}} \qquad (8)$$

Fig. 6 shows the CV loop gain for the converter in Figs. 1 and 2.

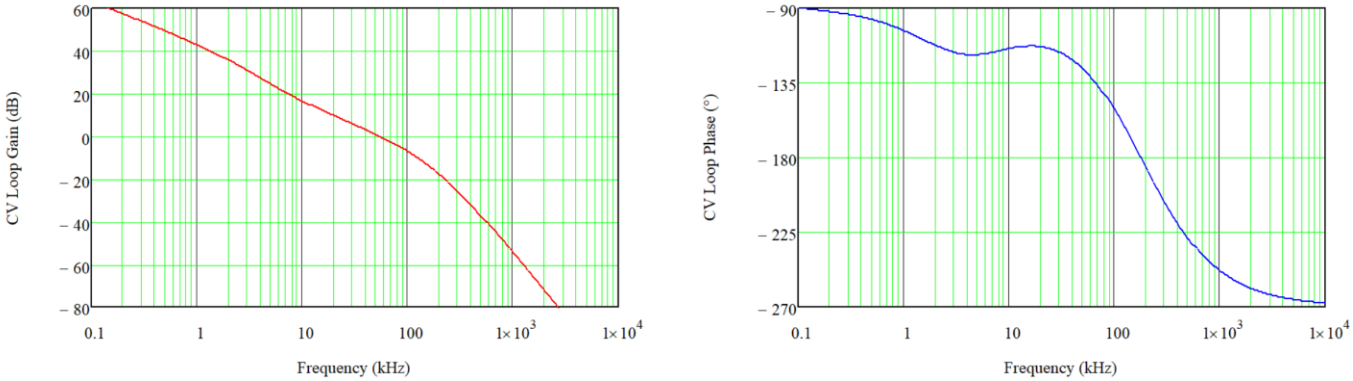

Fig. 6. Magnitude (a) and phase (b) of the CV loop gain, $T_{cv}(s)$.

Deriving The CC Loop Transfer Function

By simplifying Fig. 3, Fig. 7 represents the small-signal block diagram for the CC loop, which has an error amplifier of transconductance $g_{m\text{-}CC}$ and a compensation network impedance shared with the voltage loop.

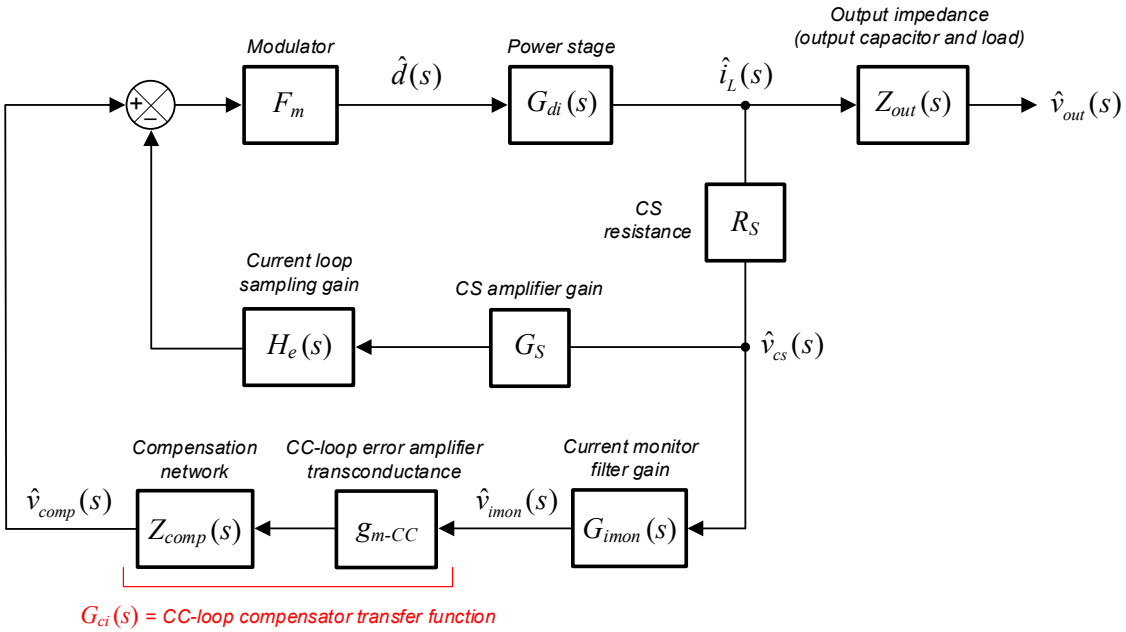

Fig. 7. Small-signal block diagram of the CC loop.

Comprising R_{imon} and C_{imon}, the IMON component network in Fig. 2 forms a pole such that equation 9 is true:

$$G_{imon}(s) = \frac{g_{m\text{-}imon} R_{imon}}{1 + sR_{imon}C_{imon}} = \frac{g_{m\text{-}imon} R_{imon}}{1 + \dfrac{s}{\omega_{p\text{-}imon}}} \qquad (9)$$

Equation 10 expresses the CC-loop compensator transfer function as

$$G_{ci}(s) = \frac{\hat{v}_{comp}(s)}{\hat{v}_{imon}(s)} = -g_{m\text{-}CC} Z_{comp}(s) \qquad (10)$$

If $G_{comp\text{-}to\text{-}vcs}(s)$ is the control-to-current-sense-voltage transfer function, using equations 4 and 6 yields

$$G_{comp\text{-}to\text{-}vcs}(s) = R_S \frac{G_{comp\text{-}to\text{-}vout}(s)}{Z_{out}(s)} = R_S \frac{\frac{R_{load}}{R_i k_d} \frac{1 + sR_{esr}C_{out}}{1 + s\frac{R_{load}C_{out}}{k_d}} H(s)}{R_{load} \frac{1 + sR_{esr}C_{out}}{1 + sR_{load}C_{out}}} = \frac{R_S}{R_i k_d} \frac{1 + sR_{load}C_{out}}{1 + s\frac{R_{load}C_{out}}{k_d}} H(s) \qquad (11)$$

or, more simply, equations 12 and 13:

$$G_{comp\text{-}to\text{-}vcs}(s) = A_{comp\text{-}to\text{-}vcs} \frac{1 + s/\omega_{z\text{-}load}}{1 + s/\omega_p} H(s) \qquad (12)$$

$$A_{comp\text{-}to\text{-}vcs} = \frac{R_S}{R_i k_d} \qquad (13)$$

Fig. 8 shows the COMP-to-VCS transfer function for the converter in Fig. 1. In this case, k_d = 1.22, and the load pole and zero are at 2.45 kHz and 2 kHz, respectively.

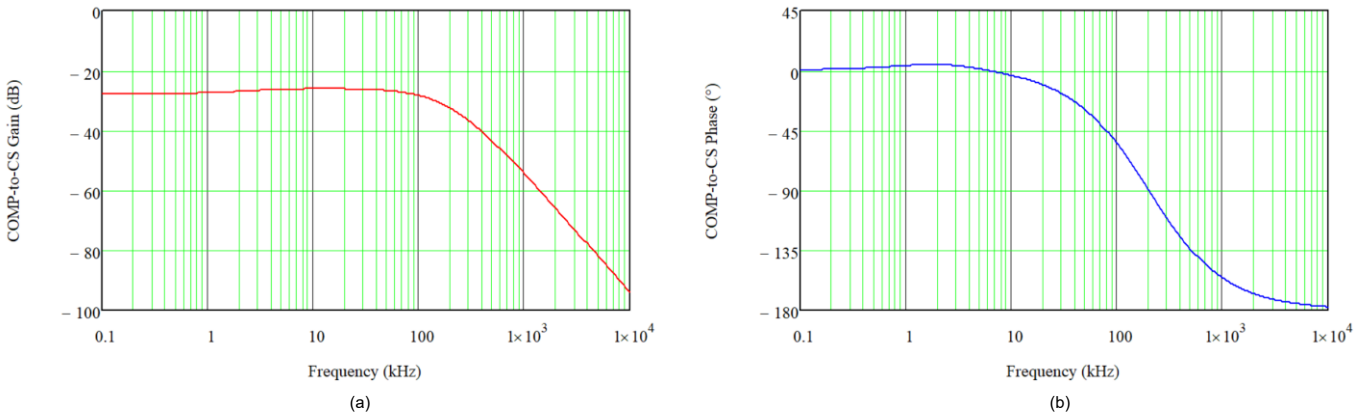

Fig. 8. Magnitude (a) and phase (b) of COMP-to-VCS response, $G_{comp\text{-}to\text{-}vcs}(s)$.

The current loop gain is the product of the VCS-to-IMON (IMON filter), IMON-to-COMP (compensator) and COMP-to-VCS (plant) transfer functions. Thus, the CC loop gain is expressed simply by

$$T_{cc}(s) = G_{ci}(s) G_{imon}(s)\ G_{comp\text{-}to\text{-}vcs}(s) = -g_{m\text{-}CC} Z_{comp}(s) \cdot \frac{g_{m\text{-}imon} R_{imon}}{1 + \frac{s}{\omega_{p\text{-}imon}}} \cdot \left[A_{comp\text{-}to\text{-}vcs} \frac{1 + \frac{s}{\omega_{z\text{-}load}}}{1 + \frac{s}{\omega_p}} H(s) \right] \qquad (14)$$

Selecting the IMON pole to cancel the load zero, the CC loop gain expression simplifies to

$$T_{cc}(s) = -A_{cc} Z_{comp}(s) \frac{1}{1+\frac{s}{\omega_p}} H(s) \qquad (15)$$

And the dc gain term is

$$A_{cc} = g_{m\text{-}CC} g_{m\text{-}imon} R_{imon} A_{comp\text{-}to\text{-}vcs} = g_{m\text{-}CC} g_{m\text{-}imon} R_{imon} \frac{R_S}{R_i k_d} \qquad (16)$$

When the CC loop engages, the voltage on the IMON resistor regulates to the CC-loop error amplifier reference voltage such that

$$V_{ref\text{-}CC} = \left(g_{m\text{-}imon} R_{imon} R_S\right) I_{out\text{-}CC} \qquad (17)$$

and thus the dc gain term becomes

$$A_{cc} = \frac{g_{m\text{-}CC}}{R_i k_d}\left(g_{m\text{-}imon} R_{imon} R_S\right) = \frac{g_{m\text{-}CC}}{R_i k_d} \frac{V_{ref\text{-}CC}}{I_{out\text{-}CC}} \qquad (18)$$

Equation 18 is of similar composition to equation 8 for A_{cv} of the CV loop.

Table 1 synopsizes the pertinent expressions for the CV and CC loops.

Table 1. CV and CC loop parameters.

Gain term	CV loop	CC loop
Control-to-output gain	$G_{comp\text{-}to\text{-}vout}(s) = A_{comp\text{-}to\text{-}vout} \frac{1+\frac{s}{\omega_{esr}}}{1+\frac{s}{\omega_p}} H(s)$	$G_{comp\text{-}to\text{-}vcs}(s) = A_{comp\text{-}to\text{-}vcs} \frac{1+\frac{s}{\omega_{z\text{-}load}}}{1+\frac{s}{\omega_p}} H(s)$
DC gain	$A_{comp\text{-}to\text{-}vout} = \frac{R_{load}}{R_i k_d}$	$A_{comp\text{-}to\text{-}vcs} = \frac{R_S}{R_i k_d}$
Loop gain	$T_{cv}(s) = -A_{cv} Z_{comp}(s) \cdot \frac{1+\frac{s}{\omega_{esr}}}{1+\frac{s}{\omega_p}} H(s)$	$T_{cc}(s) = -A_{cc} Z_{comp}(s) \frac{1}{1+\frac{s}{\omega_p}} H(s)$
DC gain	$A_{cv} = \frac{g_{m\text{-}CV}}{R_i k_d} \frac{V_{ref\text{-}CV}}{I_{out\text{-}CV}}$	$A_{cc} = \frac{g_{m\text{-}CC}}{R_i k_d} \frac{V_{ref\text{-}CC}}{I_{out\text{-}CC}}$

If using the same g_m and V_{ref} for both the voltage loop and current loop, neglecting the ESR zero, and setting the CC loop IMON pole to cancel the load zero, the CV and CV modes then have approximately the same loop transfer function. Thus, it is possible to design the small-signal dynamics of the CV and CC loops to be almost identical, and to use one compensation network to cover both operating modes.

Fig. 9 compares the CV and CC loop gains for the converter in Fig. 1. The plots largely align except at high frequency, as expected, with the ESR zero at 240 kHz in this example contributing phase lead. The plots fully align if the ESR is negligible.

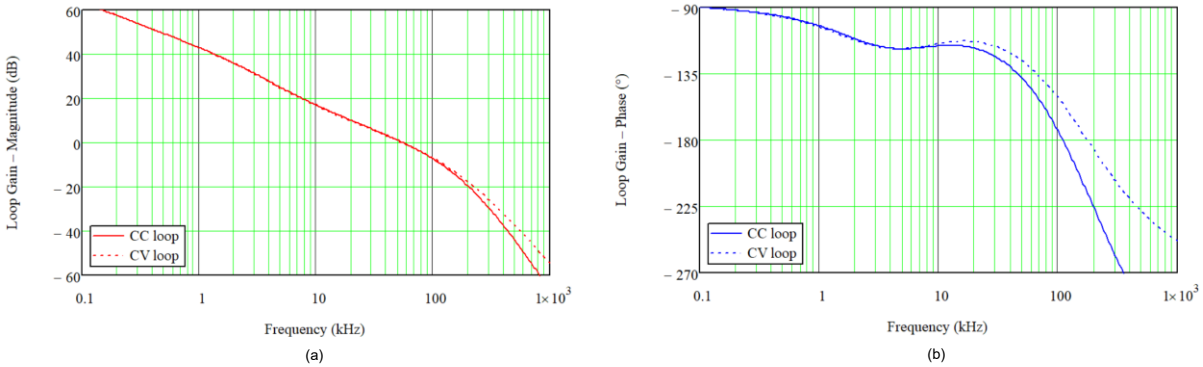

Fig. 9. Magnitude (a) and phase (b) comparison of the CV loop gain, $T_{cv}(s)$ and CC loop gain, $T_{cc}(s)$.

Circuit Simulation

Based on the converter schematic of Fig. 1 and the control circuit architecture of Fig. 2, Fig. 10 presents a SIMPLIS simulation model for a CC-CV buck converter. The element with reference designator X1 in Fig. 10 is the SIMPLIS clock edge trigger to locate the periodic operating point of the circuit before running frequency-domain analyses.

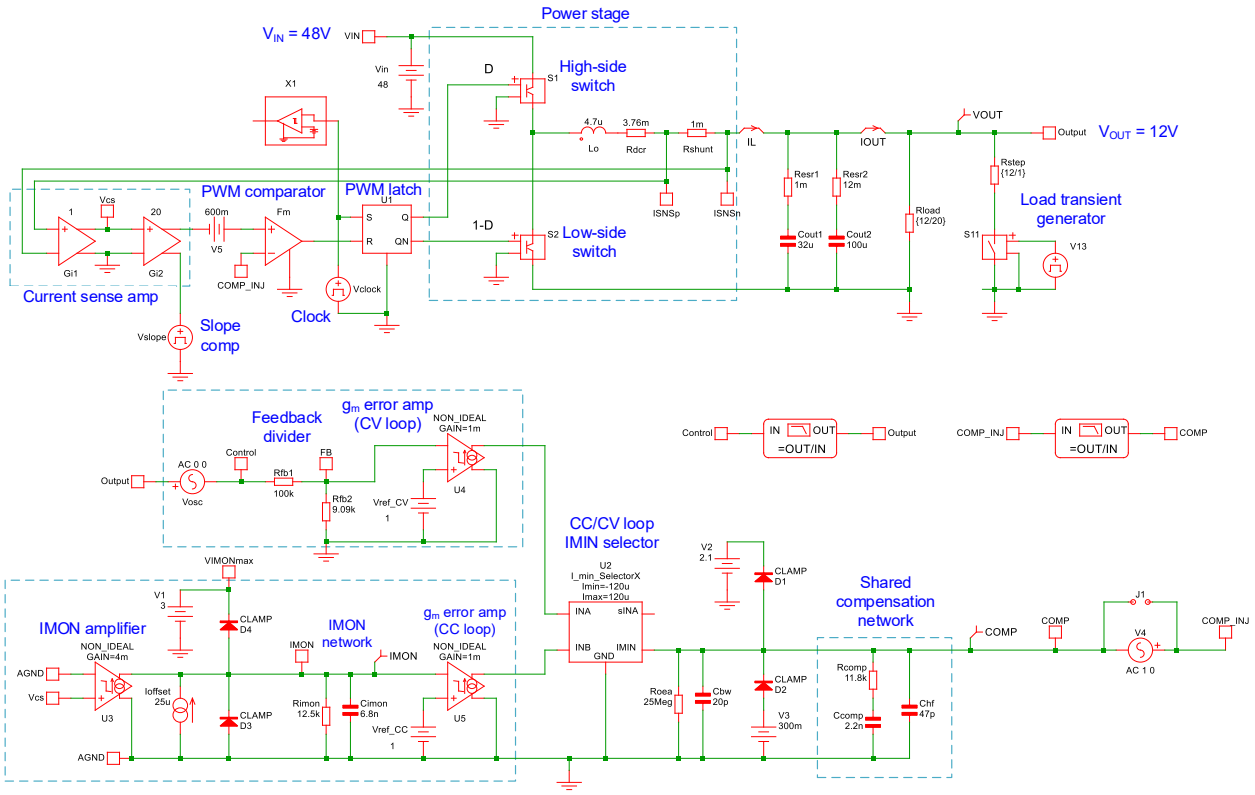

Fig. 10. SIMPLIS simulation schematic of the proposed CC-CV architecture.

Table 2 summarizes the circuit operating conditions, power-stage component values and control circuit parameters. Matching the theoretical example previously, the load in this model requires CV and CC regulation setpoints of 12 V and 20 A, respectively.

Table 2. Parameters for a CC-CV buck converter design.

Power-stage parameters				**Control-circuit parameters**			
V_{in}	48 V	L_O	4.7 µH	G_S	20	$g_{m\text{-}CV}$	1 mS
$V_{out\text{-}CV}$	12 V	R_S	1 mΩ	S_e	180 mV/µs	$g_{m\text{-}CC}$	1 mS
$I_{out\text{-}CC}$	20 A	C_{out}	132 µF	$g_{m\text{-}IMON}$	4 mS	R_{EAout}	25 MΩ
F_{SW}	400 kHz	R_{esr}	6 mΩ	I_{offset}	25 µA	C_{bw}	20 pF

Fig. 11 shows simulated Bode plots of the CV and CC loop gains, which largely align with the theoretical results of Fig. 9. Specifically, the crossover frequency and phase margin in Fig. 9 and Fig. 11 match closely, confirming the unified CC-CV loop approach. As before, the ESR zero creates a phase boost above 10 kHz. The slight phase difference between 600 Hz and 6 kHz is a result of the IMON pole not perfectly canceling the load zero in the CC loop-gain expression.

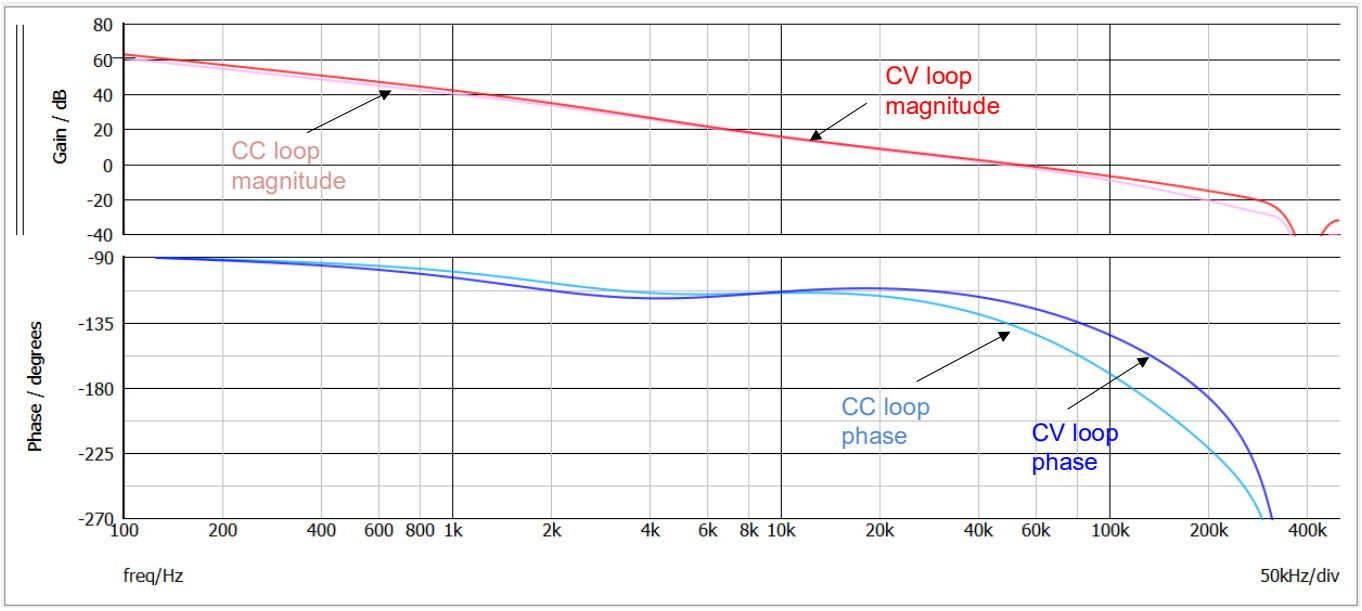

Fig. 11. Simulated Bode plots of the CV and CC loop gains, $T_{cv}(s)$ and $T_{cc}(s)$.

Summary

A primary objective of this article was to derive the small-signal response for the CC loop of a buck regulator based on a buck converter IC with an enhanced dual-loop CC-CV architecture. Results from simulation validate the theoretical analysis of the CC loop. Part 5 of this article series will examine design and performance characterization of the CC loop in a CC-CV buck regulator.

References

1. "Current Mode-Controlled DC-DC Regulators (Part 1): A Review of Small-Signal Behavior," by Timothy Hegarty, How2Power Today, November 2024.

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3. "Current Mode-Controlled DC-DC Regulators (Part 3): CC-CV Regulation," by Timothy Hegarty, How2Power Today, February 2025.
4. "LMG708B0 5V to 80V, 20A synchronous stepdown converter with integrated GaN FETs for ultra-high efficiency," product page.
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About The Author

Timothy Hegarty is a senior member technical staff (SMTS) in the Switching Regulators business unit at Texas Instruments. With over 25 years of power-management engineering experience, he has written numerous conference papers, articles, seminars, white papers, application notes and blog posts. Tim's current focus is on enabling technologies for high-frequency, low-EMI, isolated and nonisolated regulators with a wide input-voltage range, targeting industrial, enterprise and automotive applications. He is a senior member of the IEEE and a member of the IEEE Power Electronics Society.

For further reading on current-mode control, see the "How2Power Design Guide," locate the Design Area category and select Control Methods.